

# EVALUATION OF CHIP SCALE PACKAGING USING ACOUSTIC MICRO IMAGING: AN OVERVIEW OF APPLICATIONS, LIMITATIONS AND DIRECTIONS FOR FUTURE DEVELOPMENTS

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## ABSTRACT

Implementation of Chip Scale Packages in electronic products has imposed increased demands on inspection and reliability of the products. Novel technologies used in the design of the chip scale packages and compact dimensions can have potential reliability issues. Furthermore the designs require more than conventional visual inspection methods.

Although flip chips are often considered a separate category from chip scale packages, they are being included in this discussion concerning acoustic evaluation methods. Much experience has been gained concerning acoustic analyses of flip chip attach. A number of types of flip chip bonding methods have been successfully evaluated including solder bonds, gold thermal compression and anisotropic conductive adhesives. The flip chip interconnects can be analyzed for the bonding of the bumps to the chip, the bumps to the substrates, anomalies (such as voids and cracks) within the volume of the bump and passivation cracking in and around the bond pads on the chip. In some devices difficulties are encountered due to edge effects from the die when perimeter bumps are very near the edge of the die; however, information can be obtained in these areas without sample preparation. For failure analysis applications limited sample preparation such as back thinning of the die can be employed to gain better access to perimeter bumps. The underfill encapsulation can be evaluated by acoustic methods as well. In fact high volume inspection of flip chips for evaluation of voids in the underfill is being accomplished in production environments.

In some cases acoustic microscopic evaluation of chip scale packages is similar to the evaluation of related types of packages. For example, when evaluating chip scale PBGAs and TSOPs many of the principles developed for inspecting other plastic encapsulated devices can also be applied. In addition to evaluating the internal construction of components, the bonding of components to their substrates is of interest. This application is not so straightforward. The relatively complex materials and construction of the packages and the substrates are often limiting factors in gaining access to the solder joints.

The material which follows describes acoustic micro imaging and its application to flip chip and chip scale packaging.

## BACKGROUND - ACOUSTIC MICROSCOPY

For the analysis of flip chips and chip scale packages mounted to substrates a reflection mode acoustic micro imaging method is typically used. The method involves pulse-echo ultrasound typically over a range from 5 to 180 MHz to produce images of samples at specific depth levels. A focused ultrasonic transducer alternately sends pulses into and receives echoes from discontinuities within the sample. The echoes are separated in time based on the depths of the reflecting features in the sample. An electronic gate is used to select a specific depth or interface to view. A very high speed mechanical scanner is used to index the transducer across the sample and produce images in tens of seconds.

Several imaging techniques were used in the evaluation of the samples in this study. Basically, defects can be imaged at the level they occur or the influence of the defects can be detected at a subsequent interface(s). It is important to realize that when using acoustic micro imaging for evaluation of the packages and their solder joints all defects and structures at previous interfaces affect the information available at subsequent interfaces. A general discussion of the methods for evaluating devices using acoustic micro imaging follows. The specific effects of device construction on the detection of defects at the various levels will be discussed in the review of chip scale package applications.

### A-Scan

In reflection mode acoustic micro imaging the fundamental echo information is contained in what is called the A-Scan. The A-Scan is an oscilloscopic display of echo depth information in the sample at each x, y coordinate. Echoes displayed in the A-Scan correspond to different interfaces in the device being examined. The distance between the echoes relates to their depth locations. The amplitude and phase polarity information of the echoes are used to characterize the interface. The equation which describes the reflection echo amplitude at a simple interface is as follows:

$$R = I \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

Where R is the amplitude of the reflected pulse, I is the amplitude of the incident pulse,  $Z_1$  is the intrinsic acoustic impedance of the material through which the pulse is traveling and  $Z_2$  is that of the next material which is encountered by the pulse at an interface. Since a bond that is beyond the interface(s) of interest. The amount of ultrasound transmitted to the gate is analyzed. Defects at any level prior to the gate will appear as shadows as the defects block the transmission of the ultrasound to the gated level. The acoustic signal reaching the deeper level is evaluated to gain information on the condition of all the preceding bond interfaces in the sample. This method provides a shadowgraph image of the previous levels. The

between dissimilar materials gives rise to an echo signal and a disbond also gives rise to an echo signal, the challenge is to interpret the data.

### Interface Scan Technique

The most common imaging method used to evaluate devices for delaminations and voids is the interface scan. This method involves electronically gating the A-Scan signal for the appropriate echo from the interface to be investigated. The geometric focus of the acoustic beam is optimized for the interface as well. The acoustic image of an interface displays both the amplitude and phase (polarity) of the gated echoes. In this mode an image is made of just the positive echoes or just the negative echoes or both color coded within the same image.

### Loss of Echo at Back Surface

This technique is a variation of the interface scan method. However, in this case the gate is positioned to an interface high sensitivity of the technique is due to the inability of ultrasound to traverse even a small 0.1 micron air gap.

A look at the interface and loss of back surface echo methods applied to a hypothetical flip chip sample is shown in Figure 1.

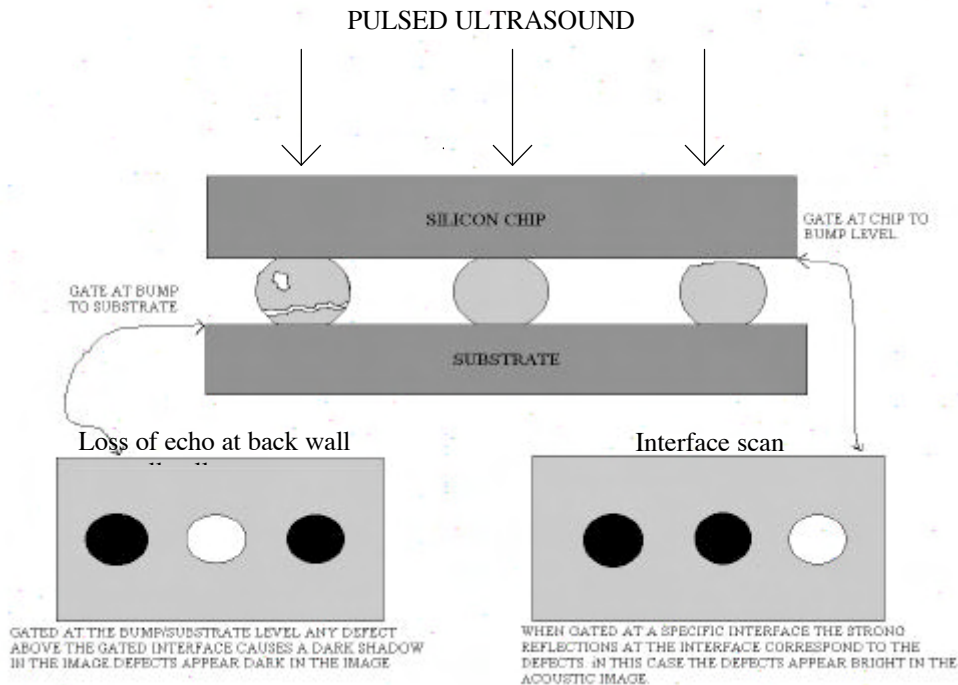
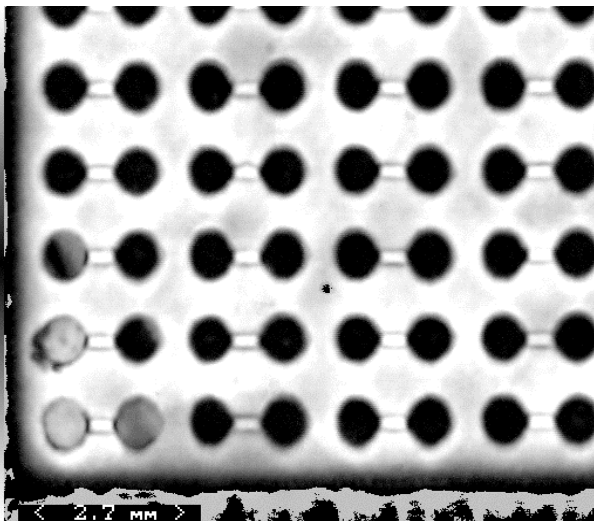
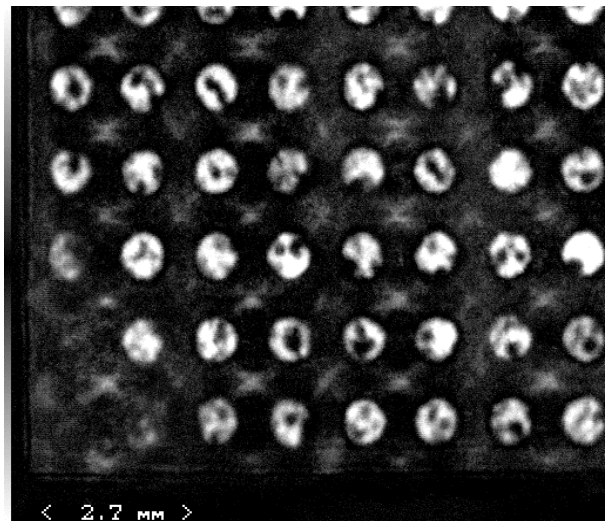


Figure 1 - Loss of echo at back surface versus interface scan. The loss of back surface echo technique will pick up defects at all levels within the interconnect but does not specify the level of the defect. The interface scan is level specific. However, defects occurring at layers below the gated region are not detected.



Ceramic to Solder



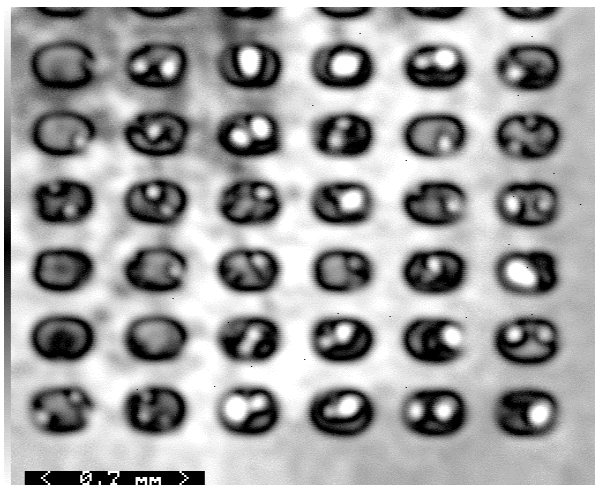
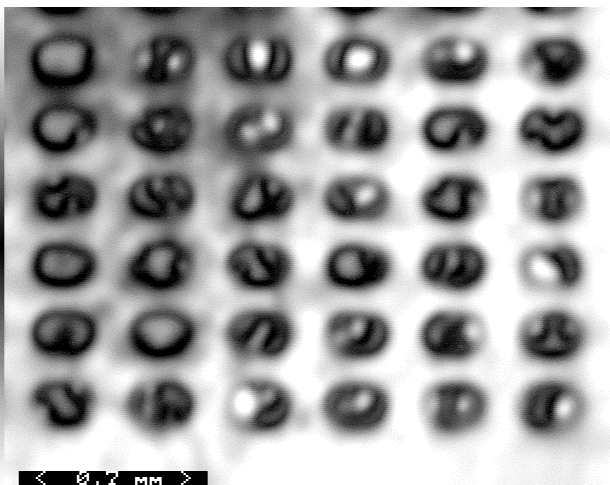
Solder Bump to PCB Substrate

Figure 2 - Acoustic images of a simple (dummy) ceramic BGA device which demonstrates the principles presented in Figure 1. At the ceramic to solder bump level disbonded bumps appear bright. Bonded bumps appear as dark circular areas. At the solder bump to PCB substrate level bumps containing no defects above the interface appear bright. Most of the bumps show smaller black areas within the bright region corresponding to the bump. The dark features indicate the presence of voids in the solder. The disbonded bumps at the ceramic/bump level appear missing from the pattern.

## FLIP CHIP INTERCONNECT EVALUATION

Flip chips are mounted circuitry side down (flipped) directly to the substrate connection sites by means of solder bumps (in most cases) or gold bumps. The devices are typically underfilled with an epoxy encapsulant to seal the device and add mechanical strength<sup>[1]</sup>. A badly bonded bump or voids within the solder can lead to electrical failure. Voids in the underfill material can also cause problems. Flip chip samples are evaluated using the reflection mode technique due to the fact that the devices are mounted, in many cases, to multi-layer substrates or composite boards. These types of substrates prohibit access to the bond interfaces of the interconnects in the through-transmission mode. The reflection mode allows for single sided access through the

back of the silicon die. Flip chip bonds are relatively small in size (typically 50 to 100 microns). This necessitates high resolution in the images in order to view the small features. The higher the ultrasonic frequency the higher the resolution in the acoustic images. As a result, there is an ongoing effort to develop increasingly higher frequency transducers to achieve the best available resolution for this application. A previous paper<sup>[2]</sup> presented early work done on acoustic evaluation of flip chips. The following examples describe more recent experiences. Figure 3 shows images of the chip to solder bump interface on a flip chip sample at two different frequencies. This example demonstrates the improvement in resolution at higher frequencies.



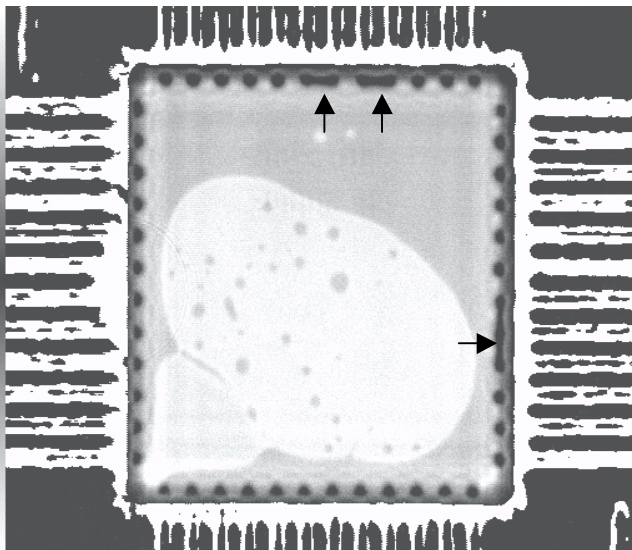
180 MHz

230 MHz

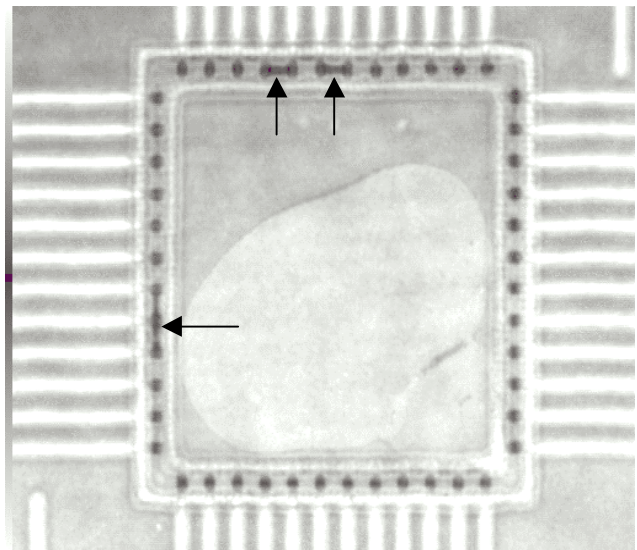
Figure 3 - Comparison of 180 MHz and 230 MHz acoustic images of flip chip bonds containing voids at the chip/bump interface. Voids at the interface appear as white features. Bonded bumps appear dark. Note the improvement in image resolution at the higher frequency.

As mentioned in the background, features and defects at a level above the interface of interest will influence the information available at this level. Therefore, it is desirable to evaluate an interface through the path which offers the least interference; for example, through the back of the die to evaluate chip to bump bonding and through the substrate to evaluate the bump to substrate interface. However, the internal construction of many substrates and, of course, PC

boards are relatively complex and multi-layered. In these instances the bump to substrate level must be accessed through the chip side of the device using the loss of echo at back surface technique. The following figures display several examples of flip chip to single layer ceramic substrates (Figures 4 & 5) and to a composite PC board (Figure 6).

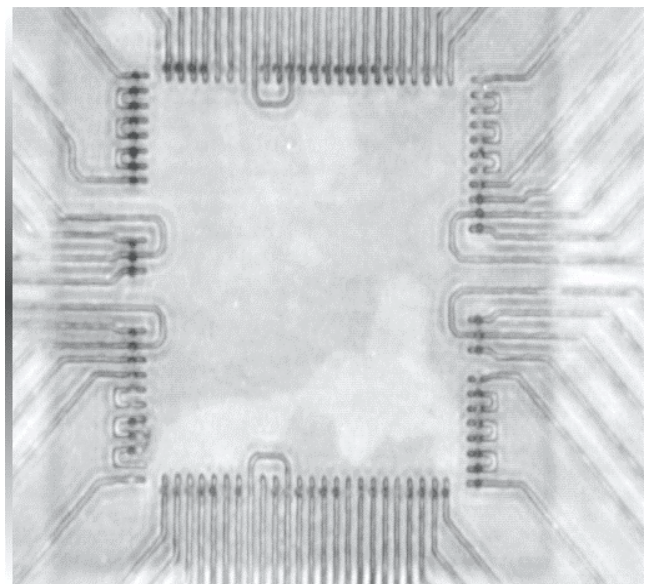
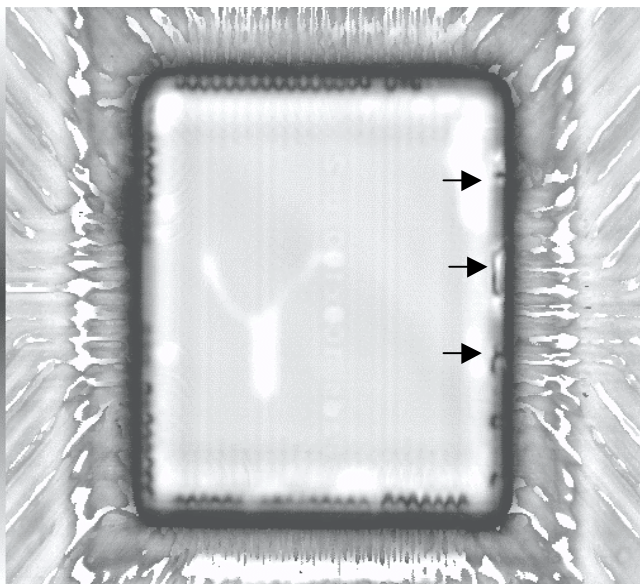


Chip/Bump Interface



Substrate/Bump Interface

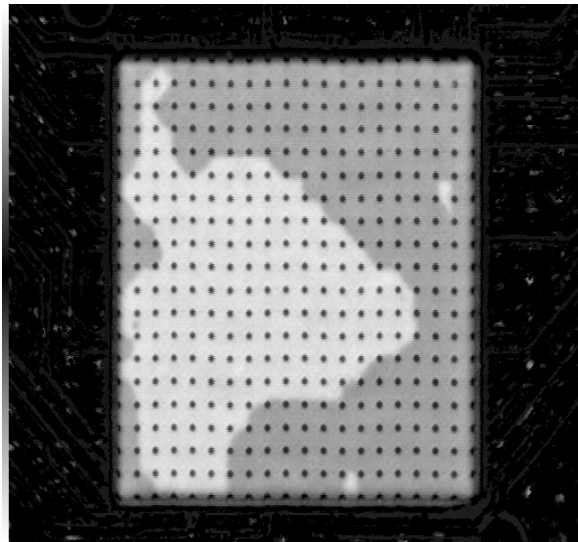
Figure 4 - Acoustic images through the chip surface and through the ceramic substrate of the same solder bonded device. Bridging of several solder bumps is present (arrows). The orientation of the sample is flipped left to right when comparing the chip/bump vs. substrate/bump interfaces.



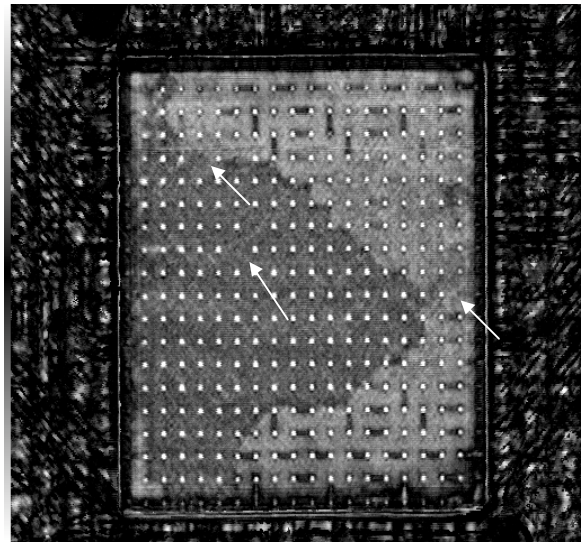
### Chip/Bump Interface

### Substrate/Bump Interface

Figure 5 - Acoustic images comparing the chip/bump to substrate/bump levels in a gold bump, thermal compression bonded sample. The orientation of the part is flipped left to right at the bump substrate level compared to the chip/bump image. The bonded solder bumps should appear as dark circles at the chip/bump level. The acoustic image shows many of the bumps to be badly bonded and cracking is observed in the surface layers of the silicon (arrows). At the substrate bump level the metallization traces on the substrate are visible. Bonded bumps appear as dark spots on the traces. Some are misaligned. In many cases the bonds are missing and show low contrast in the image blending with the appearance of the traces.



Chip to Bump



Bump to Substrate

Figure 6 - The chip to bump interface in this example of flip chip to composite PC board shows all the bumps as dark spots indicating they are bonded at this level. The bright areas indicate trapped air between the chip and the PCB. At the bump to substrate level bumps which contain no defects at the chip/bump level or within the volume of the solder bump appear bright. Several bumps appear dark (missing) from the established pattern. These are the bumps containing defects such as voids or cracks. No sound transmits through the trapped air under the chip. In the areas where the fluid couplant conducts the sound to the board level some pattern of the metallization on the PCB can be seen.

Flip chip samples which had been thermally cycled were submitted for acoustic analysis to determine if a nondestructive method could be found to locate defects in the solder joints, particularly cracks in the solder joints which were the expected mode of failure. The chip was attached to a complex multi-layer ceramic substrate which prevented access to the solder joints through the substrate side of the device. All inspection had to be through the chip side of the package. These samples were originally evaluated using 100 MHz (Figure 7a). As can be seen, the

edge bumps are present in the image; however, the image is not as clear due to edge effects from the thickness of the chip. Figure 7b shows an image of the same type of device after back thinning the die. The reduced thickness of the silicon essentially eliminates the edge effect giving a clear image of the bump bond sites nearest the edges. The thinned chip also allows for inspection of the sample using a higher frequency transducer with a high numerical aperture lens. This design of the transducer provides for higher resolution in the image.

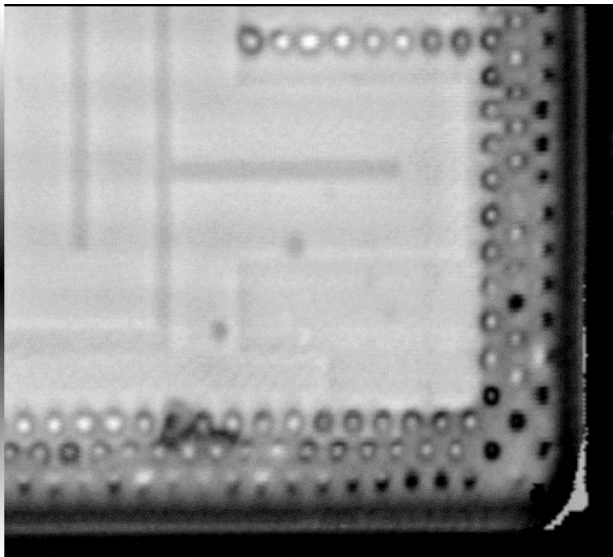


Figure 7a - 100 MHz acoustic image of chip/bond pad level using level specific imaging technique. Variations in the signal intensity are apparent from one bond site to another. The parameters for this image cause strong signal reflections characteristic of voids and delaminations to be shown in white. Dark spots (low signal reflections) indicate the bonded pads at this level.

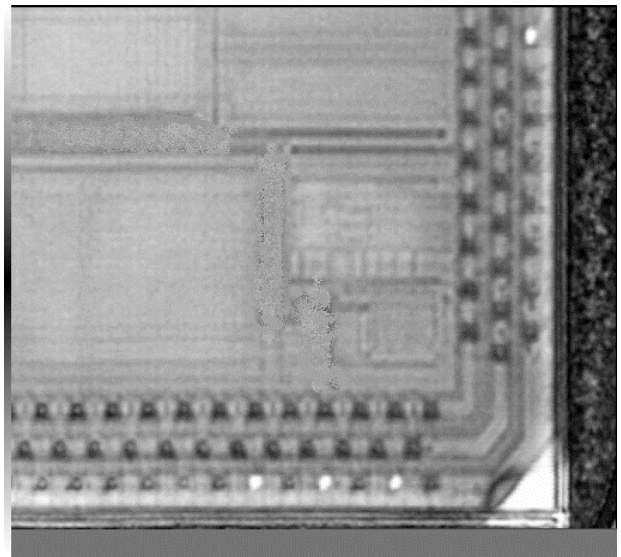


Figure 7b - High frequency acoustic image of a back thinned flip chip sample. Bumps near the edge are clearly visible as is detail of the chip metallization. Bonded bumps appear as dark spots. Several disbonded (white) bumps are present.

Underfill evaluation is also important in flip chip devices to redistribute the thermal stresses which occur during temperature cycling in the operation of the device. Voids in the underfill particularly near the bumps can lead to solder creep and an increased probability of cracks in the solder joints. Figure 8 shows an acoustic image of the underfill in a flip chip device.

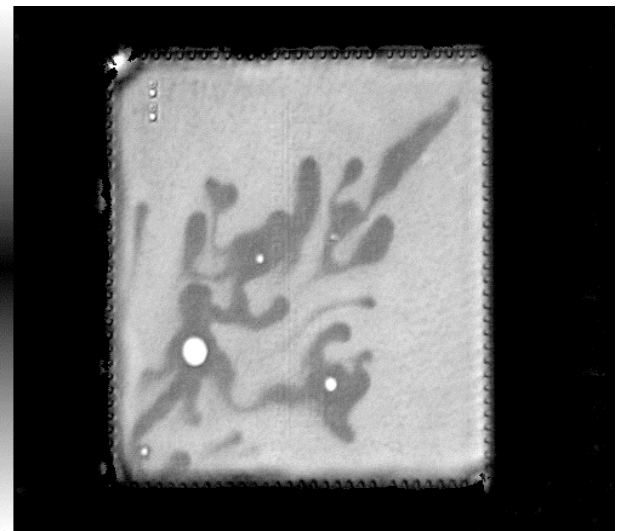


Figure 8 - An acoustic image of flip chip underfill . Voids in the underfill appear as white spots. The underfill is shown in shades of grey. The dark grey pattern within the underfill results from a segregation of filler particles in this area

### **μBGA**

μBGAs are a chip scale package which employs a flexible interposer to reroute the perimeter wire bonds to an area array pattern. Similar to flip chip, the die is circuitry side down in the package. There is an elastomer between the silicon die and the interposer. The entire package is then bonded to the substrate board. The areas of interest for evaluation are the

integrity of the internal structures of the package itself and its bonding to the substrate. The wire bonds to the chip can be evaluated through the back side of the die similar to flip chip die/bump inspection. Voids in the elastomer material can also be detected. Prior to mounting on the substrate, the interposer can be evaluated for delaminations in the multi-layer flex circuit. Evaluation of the solder bonds to the PCB is not as straightforward. These parts are typically mounted to multi-layer composite PC boards which prevents access

through the board to the solder bonds using acoustic microscopy. Signal reflection losses due to the dissimilar materials, attenuation in the elastomer material, and the intentional flexibility of the interposer cause difficulties in obtaining and gating the acoustic signal at the board level when analyzing the parts through the chip side of the package. However, some progress has been made in accessing the interposer level by using lower frequencies.

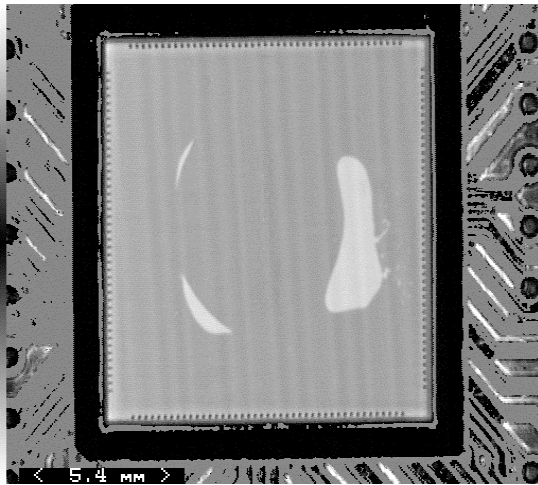


Figure 9 - 180 MHz acoustic image of  $\mu$ BGA through back of silicon die. Voids in the elastomer appear as white areas. The wire bonds appear as dark spots at the perimeter of the die in the image.

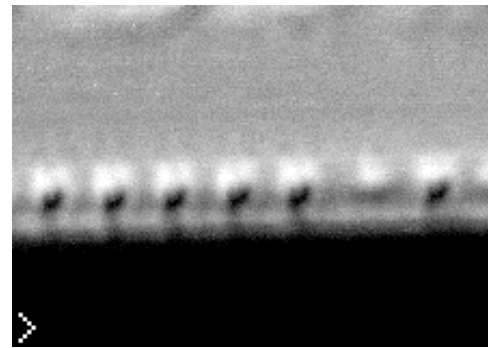


Figure 10 - Shows a high magnification view of the wire bonds on a different  $\mu$ BGA device. The wire bonds appear as dark spots within the lighter color bond pads. Notice that one of the bond pads contains no wire bond.

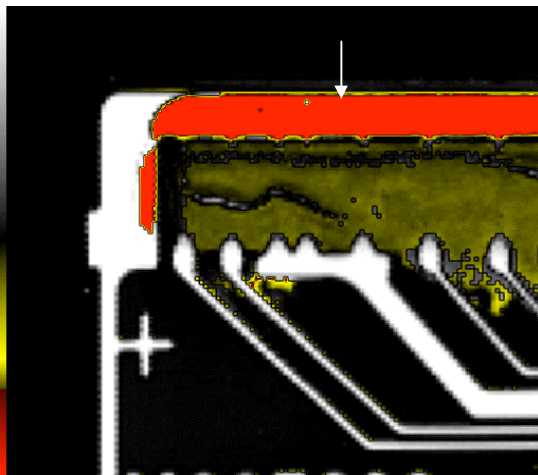


Figure 11 - A 210 MHz acoustic image of the flexible interposer shows a delamination between the polyimide and a metal trace as a red area (dark grey in the black and white reproduction). The bonded metal traces are shown in white.

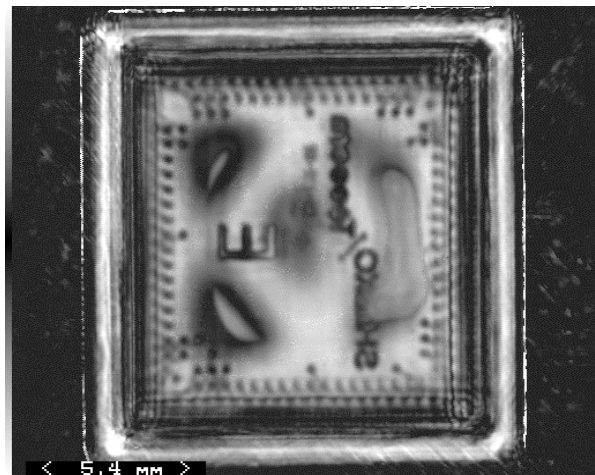


Figure 12 - Shows the metallization on the interposer including the solder bump sites through the silicon and elastomer materials.

### PBGA

These packages are essentially the same in construction as the larger BGA packages. A die is bonded to a thin multi-layer resin substrate. The package is encapsulated on the die side using plastic molding compound. The

interconnections are typically accomplished by wire bonding and the connections are routed through the resin substrate to solder connections on the back of the package substrate for attachment to the PC board. Much experience has been gained concerning acoustic inspection of these devices for internal delaminations, cracks and voids in the

packages themselves. Through-transmission imaging has proven a valuable inspection method for units which are not bonded to substrates. Again, it is the bonding to the PCB boards which poses the greatest challenge to acoustic evaluation. The complex layering of materials within the component makes access to the solder joints difficult through the component side of the packages and, similarly, the construction and composition of the PCB substrates makes access to the solder bonds difficult through the substrate. Also, any defect present within the package will prevent access to the solder bond level through the

package. But similar to the  $\mu$ BGA, lower frequencies have been used to gain information at the solder bump level. Devices with purposely implanted defects in the solder bonds have been used to optimize inspection methods for specific part types. Each part type requires its own calibration as any variation in the construction of the PBGA requires changes in the imaging parameters. At this point in time inspection of the PBGA solder joints is considered a developmental application for failure analysis or research purposes.

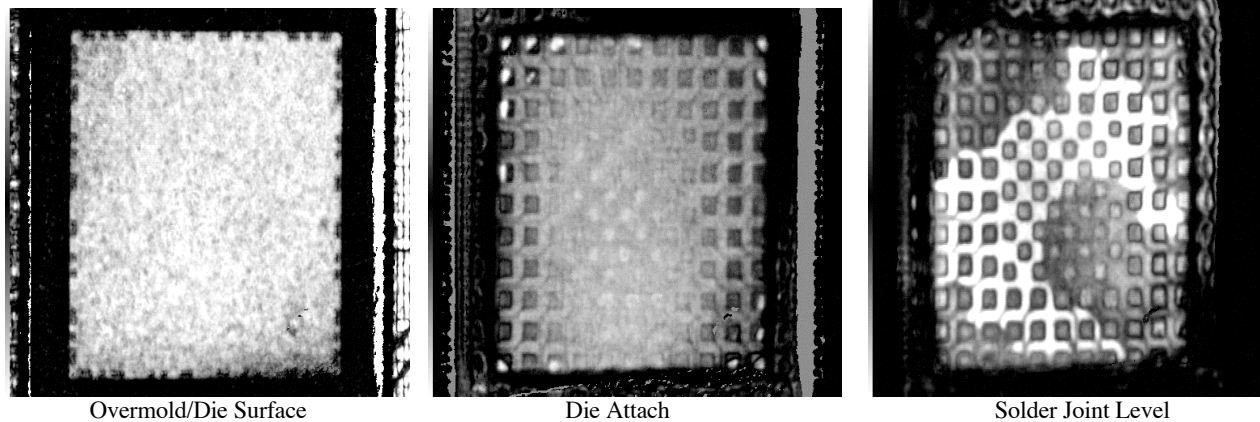


Figure 13 - The series of acoustic images display the evaluation on a chip scale PBGA. At the overmold to die interface no delaminations are detected. The wire bond sites are visible at the edges of the die. At the die attach level voids (white features) are present near the edges of the chip. At the solder joint level of the PBGA the large white area corresponds to air trapped between the device and the PCB substrate. Variations in the acoustic appearance of the solder bond sites suggest variations in the bonds but the image interpretation is not so straightforward at this level.

## CONCLUSION

Acoustic micro imaging can be successfully applied to the evaluation of chip scale packages in many instances. Clearly in the evaluation of flip chips acoustic imaging has much utility in the evaluation of both the bump bonds and the underfill. High frequencies in the neighborhood of 200 MHz are currently used to provide high resolution in the images. Analyses of other types of chip scale

packages is also possible using ultrasound particularly for the evaluation of the packages themselves for internal flaws. The evaluation of the solder bonds of these packages to PCB substrates however has proven difficult due to the complex nature of the device and board construction.

## REFERENCES

- [1] John H. Lau, "Flip Chip Technologies", McGraw Hill, 1996, pp. 25-30.
- [2] J.E. Semmens, S.R. Martell, L.W. Kessler, "Evaluation of Interconnects Using Acoustic Microscopy for Failure Analysis and Process Control Applications", 4th International Conference & Exhibition on Multichip Modules, April 19-21, 1995, Denver, CO, pp. 279-285.
- [3] O. Diaz d'Leon, M. Nassirian, R. Chowdry, "Flip Chip and BGA Failure Analysis Through Acoustic Microscopy", the 22nd International Symposium for Testing and Failure Analysis, November 18-22, 1996, Los Angeles, CA, pp. 277-283.