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Acoustic Imaging of Embedded ICs



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By Tom Adams, on behalf of Sonoscan, Inc.

EMBEDDING ACTIVE COMPONENTS WITHIN THE LAYERS OF A PRINTED WIRING BOARD (PWB) CAN DELIVER SIGNIFICANT ADVANTAGES, BUT DEVELOPING A SUCCESSFUL EMBEDDING PROCESS REQUIRES PRECISE DATA. THIS ARTICLE EXAMINES ONE COMPANY'S WORK TO PRODUCE ACOUSTIC IMAGES OF EMBEDDED ICs.

Embedding active components within the layers of a printed wiring board (PWB) can deliver significant advantages, but developing successful embedding processes requires precise data about the embedded structures. This article documents one company's* work with Fraunhofer IZM to produce acoustic images of embedded ICs.

Although the development of methods for embedding active components is still in its early stages, it is clear that one of the greatest benefits will be an increase in transmission speed. The silicon chip itself, with modified bond pads, is embedded into the PWB. In some early efforts at embedding, a cavity was cut into the PWB. In the approach described in this article, a thinned chip is bonded to the board core and laminate is laid down over the chip. One result is that the elements of the familiar IC package — epoxy molding compound, lead frame, solder joints — are no longer needed.

At the moment, no one envisions that very large boards will use embedding technologies. This technique is best suited for systems that use a maximum of one dozen ICs. Embedding ICs means that much of the board surface is free of components. Embedding both ICs and passive components can mean that the board surface is completely bare. Some passive components have been embedded for the past 30 years, but if both active and passive components are embedded, the number of solder joints is reduced to zero, making reflow unnecessary. Fraunhofer IZM is also beginning some preliminary work on embedding discrete (i.e., non-printed) passive components.

This scenario may be a trifle ambitious, but at least one product using an embedded active component is in production. While embedding active components may confer strong advantages, there are drawbacks. The most significant of which may be that rework

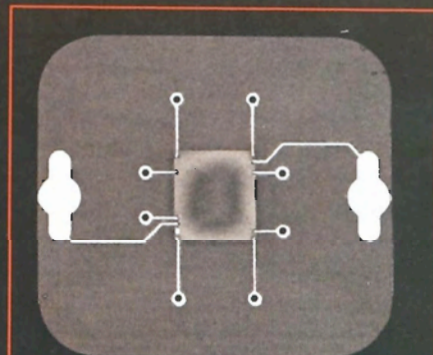


Figure 1. Planar acoustic image gated and focused below the top surface of an embedded assembly. Traces, thru-holes, and the 50- μ m-thick chip are seen at this depth.

becomes essentially impossible; a board having an embedded defect will probably be scrapped. But the same packaging integrity that precludes rework also means that systems using the embedded approach probably will be resistant

to shock, vibration, and other environmental perils. In some applications, of course, embedding may be used along with surface mounting as a way to take advantage of 3-D integration to pack maximum performance into the smallest possible volume.

The Embedding Method

The European project investigating ways to embed active devices is part of a consortium called HIDING DIES (www.hidingdies.net), which includes Nokia (Finland), Philips (Netherlands), AT&S (Austria), Datacon (Austria), CWM (Germany), IMEC (Belgium), and Fraunhofer IZM/TUB (Germany). In this project, the thinned die is attached to a board, and a layer of additional material is laminated onto the board. The laminate consists of a compliant material that will flow laterally enough to accommodate the die and produce the desired flat board surface.

The core board material is FR-4 modified, so it possesses a glass transition (T_g) temperature of 170°C, rather than the conventional 140°C. If surface mounted components are added after embedding, the higher T_g permits the board to pass without damage through lead-free reflow. Development has used core thicknesses ranging from 100 μm to 1.5 mm.

Thinning of the die to 50 μm is done at the wafer level. The aluminum contact pads are also modified at this level, making them suitable for PCB metallization. The pads are sputtered with a 0.2- μm layer of Ti/W/Cu, which is then reinforced by the electroless deposition of an additional 5 μm of copper. A purely electroless copper-bumping process is being developed. The dies typically are thinned to 50 μm , and then they are bonded adhesively to the core with an ordinary chip bonder using either printed adhesive or die-attach film. One of the goals of the project is to use existing production equipment in development work, rather than require expensive new equipment.

Next, a layer of resin-coated copper (RCC) is laminated over the chip and the surrounding board. The RCC typically is 80- μm thick, but the resin is compliant enough to accommodate the 50- μm -thick chip, as well as the modified contact pads; therefore, the top surface is very level. After the resin has been cured, a laser is used to drill microvias down to the contact pads. The microvias are then plated with copper.

Acoustic Imaging

The purpose of acoustic imaging was twofold: establish that the board was compatible with acoustic imaging, and that the various depths within the assembly could be accessed acoustically and imaged; and examine the various depths and structures for anomalies that may have occurred during assembly and processing. Early work showed that the assembly transmitted ultrasound well, so transducers with fairly high frequencies (typically 230 MHz or higher) and high resolution were used. Even though the entire assembly has a thickness of about 150 μm , careful gating of return echo signals was used to identify and separate specific depths of interest.

Figure 1 shows a planar-acoustic image gated below the top surface of the assembly. The chip, traces, and thru-holes are visible. There is some apparent irregularity in the area of the die, but this irregularity is not well defined at this imaging

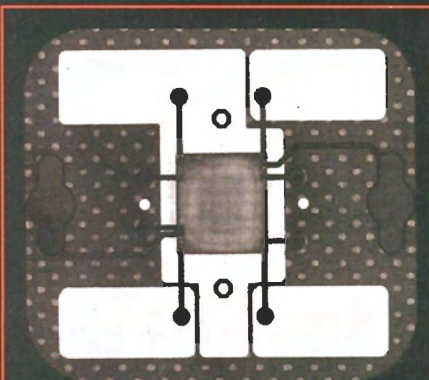


Figure 2. Planar acoustic image gated and focused at the depth of the chip attach to the board core. The only anomalous feature is some irregularity in the adhesive layer; there are no delaminations, voids, or other defects.

depth. No other anomalies are apparent. Figure 2 shows a chip that is gated at the depth of the attachment of the die to the core board material. The rounded white rectangles are copper on the surface of the core. The irregularity within the area of the die can be discerned as differential reflectivity within the adhesive material. Although anomalous, this is not of real concern as a possible defect. There are no voids, delaminations, or other features that might cause electrical failure. Some of the patterning on the die can also be seen.

Figure 3 shows a 3-D acoustic image made by collecting the return-echo signals at multiple depths and assembling this data into an electronic acoustic

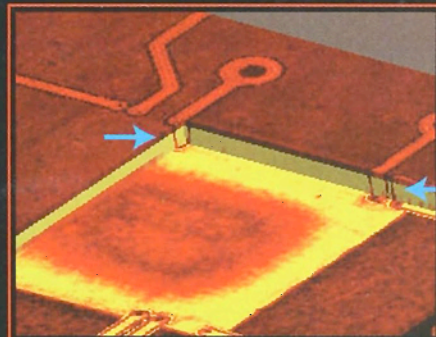


Figure 3. 3-D acoustic view in which a corner section has been removed to show in cross-section two plated microvias (arrows) leading from the top surface of the modified contact pads on the chip.

solid that can be rotated and dissected. A near-surface corner section has been removed to reveal (among other features) the cross-sectional view of the microvias leading from the top surface down to the modified contact pads on the die. Two microvias (arrows) are seen here, and their profiles show that they are only slightly tapered from top to bottom. There is some heightened reflectivity (small irregular red area) at the bottom of the right-hand microvia; this area might be of concern. The irregular structure of the adhesive material beneath the die is seen in greater detail.

Conclusion

No one knows how widely used the technique of embedding active chips may someday become. Because they make high-processing speeds possible in small, lightweight packages, they could conceivably be useful in navigation systems for small missiles or for ordnance. Embedded die can be expected to be resistant to shock and vibration, although no testing has been performed. They may also find their way into high-volume consumer applications. In tests at Fraunhofer IZM/TU Berlin, embedded chips have survived 1,000 hours of standard humidity testing and 2,000 cycles of thermal testing (-55°C/+125°C) without failure. Whatever the future of embedded active components, their response to high-resolution acoustic imaging means that it will be less difficult to achieve the high reliability that will be required. *SMT*
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